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**CHIPVISION BREAKTHROUGH ESL TECHNOLOGY ENABLES INTERACTIVE
CREATION OF RTL CODE OPTIMIZED FOR LOW-POWER CONSUMPTION**

*Achieves up to 75 percent power savings in critical semiconductor blocks;
significantly reduces development costs and design risk*

OLDENBURG, Germany and SAN JOSE, Calif. – May 14, 2007 – ChipVision Design Systems, the low-power specialist in electronic design automation, today announced breakthrough, patented Electronic System Level (ESL) technology that lets RTL designers work interactively with system-level descriptions to generate power-optimized Register Transfer Level (RTL) code. It creates implementation trade-off options for RTL designers, and immediately and accurately implements their visualized choices. Using this technology at the system level to analyze power can result in pre-RTL energy savings of up to 75 percent, shorten time-to-results by a factor of 60, and create code that is nine times more compact. It reduces development costs by achieving results far faster than other lower-level methods. It also greatly minimizes risk because designers can explore multiple options prior to hardware design – when the impact on power reduction is the greatest – and select the most appropriate path for meeting power budgets. This new technology optimizes for area and performance, as well as for power, and is ideal for companies developing mobile communications, networking, consumer and automotive applications. ChipVision expects to deliver a product based on this technology later this year, and will demonstrate the software at the 44th annual Design Automation Conference, in San Diego, June 4-8, 2007, at booth #6378.

Performs synthesis, analysis and estimation

Using a unique approach, ChipVision's new technology accepts a synthesizable subset of SystemC or ANSI C as an executable specification. A power library is generated once, automatically, from the targeted design technology, and utilized. Once the source code is imported, a pre-implementation activity profile is generated – an essential step for dynamic power analysis. The technology then enables interactive synthesis in which users control power, area, and timing trade-offs. The resulting output is an optimized architecture in the form of synthesizable Verilog code. At this stage, the RTL design team can begin the engineering change process and modify the code as desired. This technology closes the gap between system-level and RTL and, in addition, outputs constraints in Common Power Format (CPF) and Unified Power Format (UPF). It also implements leakage strategies, using technology-driven modeling for process, temperature, and voltage variations.

Low-power design has been a major design challenge for mobile and wireless applications. Optimizing for power at the architectural level rather than the gate level with ESL solutions gives companies the potential for far greater power savings. By evaluating many more architectural tradeoffs in time for remedial action, companies can anticipate achieving truly optimized power implementation.

According to Thomas Blaesi, chief executive officer of ChipVision, "Our customers tell us that power optimization rapidly is becoming a key enabler for them to achieve substantial savings in their design flows. Knowing about power design early on – in addition to timing and area possibilities – eliminates their need to wait until silicon to figure it out. The higher the level of abstraction, the larger their potential for savings and for reducing the risk of failure. I am pleased that ChipVision's power optimization technology makes the exploration of various architectures far more productive."

About ChipVision Design Systems

ChipVision Design Systems is the leading supplier of low-power system-level EDA software tools and services. Its patented software enables semiconductor developers to estimate and optimize energy dissipation in critical blocks of their design; the software

interactively creates RTL code optimized for power, performance and area. This electronic system-level (ESL) approach results in significant energy and time savings. The company's solutions are based on open industry standards including SystemC. ChipVision is headquartered in Oldenburg, Germany, and has offices in Munich and San Jose, Calif. For more information about ChipVision, its products and services, visit www.chipvision.com.

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